IN THE CLAIMS

1. (original) A semiconductor chip having a body with oppositely-directed front and rear surfaces, contacts on said front surface and internal components within said body electrically connected to said contacts on said front surface, said chip also having pads on said rear surface electrically isolated from said internal components and traces on said rear surface electrically connected to said pads.

2. (original) A chip as claimed in claim 1 wherein said internal components include active devices.

3. (original) A chip as claimed in claim 1 wherein said internal components consist only of passive devices.

4. (original) A chip as claimed in claim 1 wherein said body has edges bounding said front and rear surfaces and said traces include bonding points disposed in the vicinity of said edges.

5. (original) A chip assembly comprising:

(a) a first semiconductor chip including a first body with oppositely-directed front and rear surfaces, said first semiconductor chip having internal components within said first body, contacts on the front surface connected to said internal components, said first semiconductor chip also having pads on the rear surface of said first body and traces extending from said pads along the rear surface of the first body;

(b) a second semiconductor chip including a second body with oppositely-directed front and rear surfaces, said second semiconductor chip having internal components within the second body and contacts on the front surface of the second semiconductor chip,

said second semiconductor chip being mounted on said first semiconductor chip so that said second semiconductor chip overlies said rear surface of said first semiconductor chip, said contacts of said second semiconductor chip being electrically connected to said pads of said first semiconductor chip.

6. (original) A chip assembly as claimed in claim 5 wherein said front surface of said second semiconductor chip confronts said rear surface of said first semiconductor chip.

7. (original) A chip assembly as claimed in claim 6 wherein said contacts of said second semiconductor chip are bonded to said pads of said first semiconductor chip by masses of electrically conductive bonding material.

8. (currently amended) A chip assembly as claimed in claim 5 or claim ~~claims~~ 6 or claim 7 further comprising a substrate, said chips being mounted on said substrate with said front surface of said first semiconductor chip facing toward said substrate, said contacts of said first semiconductor chip being electrically connected to said substrate, said traces of said first semiconductor chip also being electrically connected to said substrate so that said contacts of said second semiconductor chip are connected to said substrate through said pads and traces of said first semiconductor chip.

9. (original) A chip assembly as claimed in claim 8 further bonding wires extending between said traces and said substrate, said traces being electrically connected to said substrate through said bonding wires.

10. (original) A chip assembly as claimed in claim 9 wherein said first semiconductor chip has edges bounding said front and

rear surfaces of said first body, and wherein said bonding wires are connected to said traces adjacent said edges.

11. (original) A chip assembly as claimed in claim 8 wherein said contacts of said first semiconductor chip are connected to said substrate by masses of bonding material disposed between said contacts of said first semiconductor chip and said substrate.

12. (original) A chip assembly as claimed in claim 8 wherein said contacts of said first semiconductor chip are connected to said substrate by leads extending between said contacts of said first semiconductor chip and said substrate.

13. (original) A chip assembly as claimed in claim 8 wherein said substrate is a package substrate adapted for mounting on a circuit panel.

14. (original) A chip assembly as claimed in claim 13 wherein said substrate has terminals adapted for connection to a circuit panel, said terminals being movable with respect to said first semiconductor chip.

15. (original) A chip assembly as claimed in claim 8 wherein said second semiconductor chip has pads and traces on the rear surface of said second body, the traces of said second semiconductor chip being electrically connected to said substrate, the assembly further comprising a third semiconductor chip overlying said rear surface of said second semiconductor chip and electrically connected to said pads of said second semiconductor chip.

16. (withdrawn) A method of making a semiconductor chip assembly comprising the steps of:

(a) mounting a first semiconductor chip to a substrate so that a front surface of the first semiconductor chip faces toward the substrate and a rear surface of the first semiconductor chip faces away from the substrate, and so that terminals of the first semiconductor chip on the front surface thereof are electrically connected to the substrate;

(b) making electrical connections between traces on the rear surface of the first semiconductor chip and the substrate to thereby connect pads on the rear surface of the first semiconductor chip with the substrate; and

(c) mounting a second semiconductor chip to the first semiconductor chip so that contacts of the second semiconductor chip are electrically connected to the pads of the first semiconductor chip, whereby the second semiconductor chip is connected to the substrate through the pads and traces on the rear surface of the first semiconductor chip.

17. (withdrawn) A method as claimed in claim 16 wherein said step of making electrical connections includes wire-bonding the traces of the first semiconductor chip to the substrate.

18. (withdrawn) A method as claimed in claim 17 wherein said wire-bonding step is performed before mounting the second semiconductor chip on the first semiconductor chip.

19. (withdrawn) A method as claimed in claim 18 wherein said second semiconductor chip has said contacts on a front surface and said step of mounting the second semiconductor chip on the first semiconductor chip is performed so that said front surface of said second semiconductor chip confronts said rear surface of said first semiconductor chip.